AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

At page 1, please replace the paragraph beginning at line 4 with the following paragraph:

--This application is related to co-pending and commonly assigned U.S. Patent Application to J. Culler, which was filed contemporaneously with this application and entitled SYSTEM AND METHOD FOR WAVEFORM SAMPLING, Application Serial No. 10/699,909, which was filed November 3, 2003 ~~Attorney Docket No. 200310794-1~~, the disclosure of which is incorporated herein by reference.--

--FIG. 8 is a flow diagram illustrating a methodology for synchronizing devices.--

Please replace the first full paragraph on page 6, beginning at line 5, with the following paragraph:

--The oscillator/control system 66 can be configured to adjust the frequency of the INTERNAL CLOCK signal by switching in or out one or more components based on the comparator output signal 68. For example, the oscillator/control ~~signal~~ system 66 can decrease the frequency of the internal clock signal by adding delay elements into the path of the INTERNAL CLOCK signal. In contrast, the oscillator/control system 66 can remove delay elements to increase the frequency of the INTERNAL CLOCK signal. Thus, the oscillator/control system provides means for controlling an oscillator to adjust the frequency of the internal clock signal based on the comparator output signal 68.--

Please replace the last paragraph on page 8, beginning at line 26, with the following paragraph:

--The oscillator control block 126 receives the latched UP/DN signal and a NO CHANGE signal. The NO CHANGE signal corresponds to control data indicating that no change to the CLOCK signal is required. While the UP/DN signal and the NO CHANGE signal are depicted as separate signals provided to the oscillator control block 126, a single multi-bit signal can be utilized, such as provided through the latch 124. The oscillator control block 126 controls a clock oscillator 128 based on the latched UP/DN and NO CHANGE signals. Thus, the oscillator control block 126 provides means for controlling the oscillator 128 to adjust the frequency of the internal clock signal based on the latched UP/DN and NO CHANGE signals, which as mentioned above, can be based on a comparison of frequency information for the CLOCK signal and frequency information for an external reference signal. For example, the oscillator control block 126 provides multi-bit data to the clock oscillator 128. The control data, for example, may result in one or more components being selectively switched into and/or out of the clock oscillator 128. The clock oscillator 128 in turn provides the CLOCK signal with a frequency based on the control data provided by the oscillator control block 126.--